

Electrical Characteristics of Metal Catalyst-Assisted Etched Rough Silicon Nanowire Depending on the Diameter Size

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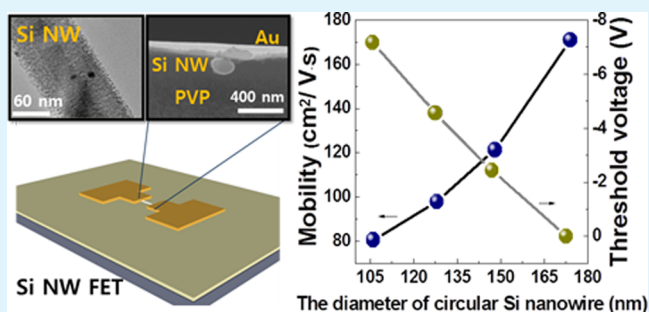
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S Supporting Information

ABSTRACT: The dependence of electrical properties of rough and cylindrical Si nanowires (NWs) synthesized by diameter-controllable metal catalyst-assisted etching (MCE) on the size of the NW's diameter was demonstrated. Using a decal-printing and transfer process assisted by Al₂O₃ sacrificial layer, the Si NW field effect transistor (FET) embedded in a polyvinylphenol adhesive and dielectric layer were fabricated. As the diameter of Si NW increased, the mobility of FET increased from 80.51 to 170.95 cm²/V·s and the threshold voltage moved from -7.17 to 0 V because phonon–electron wave function overlaps, surface scattering, and defect scattering decreased and gate coupling increased as the ratio of surface-to-volume got reduced.

KEYWORDS: silicon nanowires, diameter modulation, transfer method, field effect transistor, dielectrophoretic alignment



1. INTRODUCTION

Silicon nanowires (Si NWs) have been widely studied as building blocks for nanoscale semiconductor devices, such as field effect transistors (FETs),^{1–4} photosensors,⁵ solar cells,^{6–10} biosensors,^{11–14} and light-emitting diodes.^{15–17} Two approaches for the synthesis of Si NWs have been developed: the vapor–liquid–solid (VLS) and the metal catalyst assisted etching (MCE) method.^{18–22}

The VLS method is one of the most commonly used bottom-up routes; when this method is used, the diameter of NWs can be controlled by modulating the size of seed particles, and doped NWs can be obtained by adding the selected species in the precursor gas.²³ A variety of Si NWs synthesized through the VLS method have been already experimentally and theoretically studied and reported.^{24,25} However, NWs obtained through VLS are compositionally contaminated by the carbonaceous byproducts originating from metal–organic precursors or by seed metal elements.^{26,27} In addition, the elemental metal seed diffuses into the NWs during their growth, acting as an impurity. In case of Si NWs, Au used as a metal seed element intrudes into the NWs and acts as a deep level acceptor. This chemical contamination has detrimental effects on the device performance.^{28–30}

On the other hand, when the MCE method is used, Si NWs are directly formed from a Si wafer, without any contamination and with a uniform distribution of dopant. However, the surface properties of Si NWs synthesized using the MCE methods have not been thoroughly investigated so far. Si NWs achieved by MCE show a rougher surface than those synthesized by VLS; it

is commonly believed that superficial defects and dangling bonds may degrade the properties of devices based on Si NWs. In particular, since Si NWs present a higher surface-to-volume ratio when they are characterized by a reduced diameter, the surface roughness of NWs dominantly affects the device properties and they could be changed by the circumstance surrounding NWs. In the present study, we fabricated FETs using the rough Si NWs synthesized through the MCE process and we investigate that the electrical properties of transistor can be modulated by controlling the diameter of a cylindrical Si NW. The rough Si NWs were synthesized by using our previously reported MCE process,³¹ which allows to modulate the NW diameter without the need of any lithographic technique. To fabricate the Si NW-based transistor, each NW was addressed onto the electrodes by dielectrophoretic (DEP) alignment method on Al₂O₃ film, used as a sacrificial transfer layer, and then, each NW was printed on poly(vinylphenol) (PVP), used as an adhesive and dielectric layer.

2. RESULTS AND DISCUSSION

A four-step method for the fabrication of a Si NWs FET by direct printing using Al₂O₃ as a sacrificial transfer layer is illustrated in Scheme 1. In the first step, p-type cylindrical Si NWs were synthesized by using the MCE method allowing to control their diameter and then stored in 99.9% ethanol

Received: October 28, 2014

Accepted: December 19, 2014

Published: December 19, 2014

Scheme 1. Process Flow Sequence to Decal-Printing and Fabrication of Cylindrical-Shaped Si NWs FET Using Al_2O_3 Layer As a Sacrificial Transfer Layer

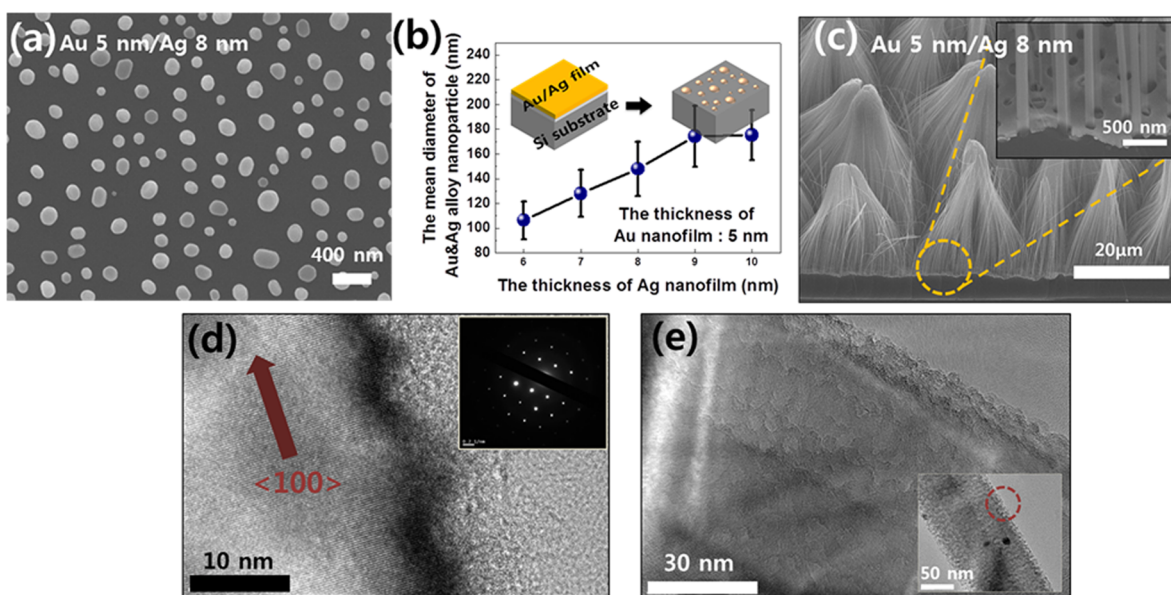
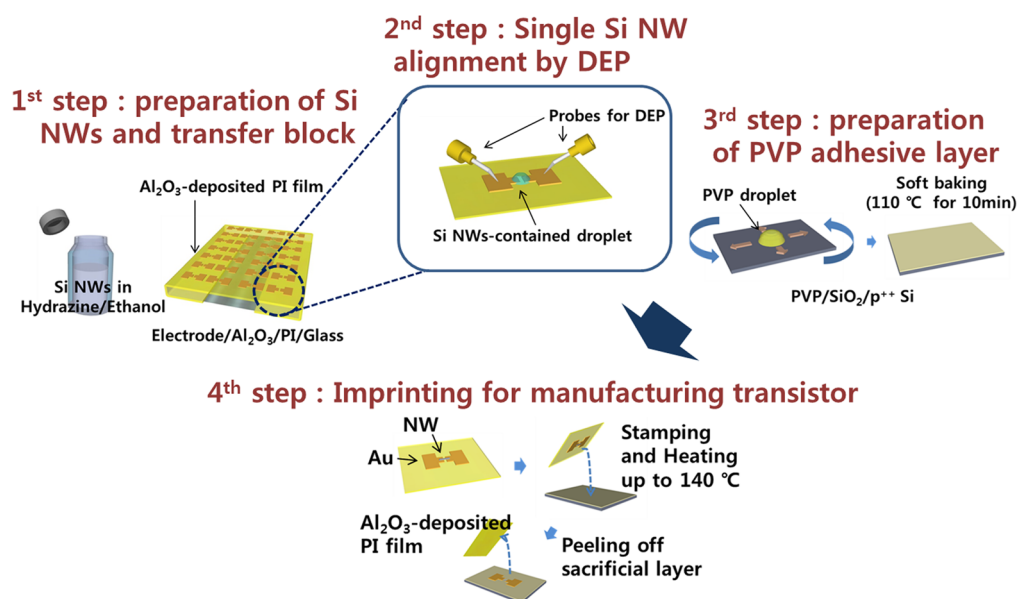


Figure 1. Formation of Au and Ag alloy nanoparticles in various thickness of Ag layer and synthesized cylindrical Si NWs. (a) A top view SEM image of Au and Ag alloy nanoparticles after rapid thermal annealing with 5 nm/8 nm in the thickness of Au/Ag layers. (b) The relationship between the Ag thickness and the nanoparticle diameter after annealing. (c) 45°-tilted SEM images of typical Si NWs formed with 5 and 8 nm in the thickness of Au/Ag layers and the shows a magnified SEM image of the circle area. (d) A TEM image of a single-crystalline with $\langle 100 \rangle$ direction. (e) Rough surface of cylindrical Si NW synthesized by MCE process.

solution. Au electrodes were defined on Al_2O_3 -coated flexible polyimide (PI) substrates by photolithography. In the second step, the Si NWs were addressed onto the Au electrodes by DEP alignment. In the third and the fourth steps, the Si NWs addressed onto the Au electrodes were decal-printed on a PVP adhesive layer, which was previously spin-coated on a commercial p⁺⁺ Si wafer with a 300 nm-thick SiO_2 layer and soft baked at 110°C for 10 min. Finally, the cylindrical Si NW FETs were completed.

Figure 1a shows a scanning electron microscopy (SEM) image of Au/Ag alloy nanoparticles on Si substrates after annealing, with the original Au and Ag film thicknesses of 5 and

8 nm, respectively. When the Ag thin film deposited on Si substrate is annealed by rapid thermal annealing (RTA), the Ag nanoparticles, which present a poor adhesion to the substrate, tend to move across the surface during etching process, resulting in coalescence phenomena. Thus, in the present work, the Au film was additionally deposited onto the Ag film and the annealing was conducted to form Au/Ag alloy nanoparticles. According to the phase diagrams of Ag–Si and Au–Si, the Ag–Si eutectic temperature is beyond the RTA temperature, which is 700°C , whereas the Au–Si eutectic reaction occurs under this temperature, so that the adhesion force between the nanoparticles and the Si substrate is enhanced.^{32,33} Figure 1b

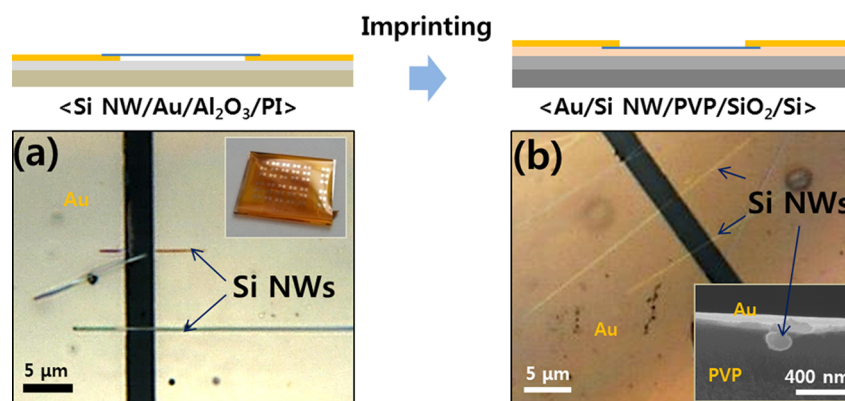


Figure 2. DEP and imprinting processes for transistor fabrication. (a) An OM image of Si NWs addressed on Au electrodes by DEP process and the inset is the digital photo image of a sacrificial transfer specimen. (b) An OM image of the transferred Si NWs and Au electrodes on to PVP adhesive layer; inset is the cross-sectional SEM image of Si NWs embedded in PVP layer and Au electrodes on it.

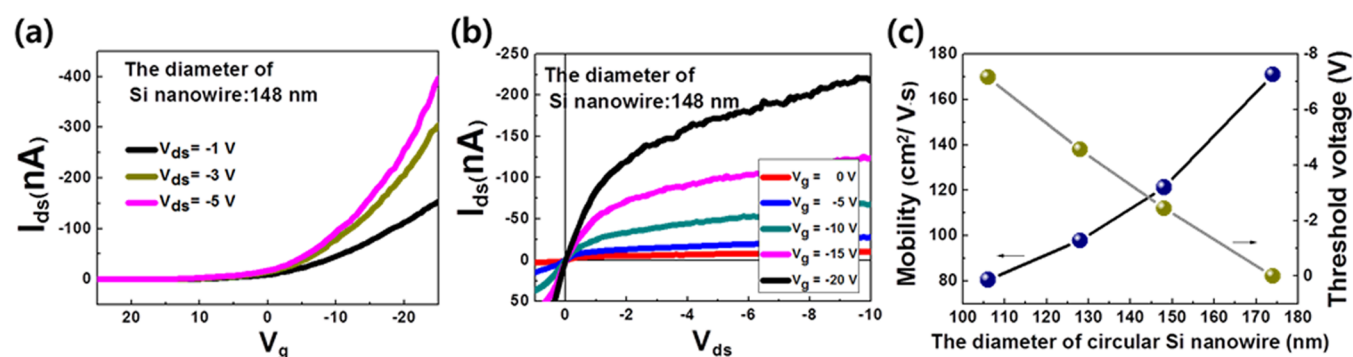


Figure 3. Electrical properties of imprinted single cylindrical Si NW FET. (a) Transfer and (b) output characteristics of the Si NW transistor with diameter of 148 nm. (c) Mobility and threshold voltage change as a function of the diameter of cylindrical Si NW.

shows that cylindrical Si NWs synthesized from Au/Ag films with a thickness of 5 and 6 nm, respectively, resulted in a mean nanoparticle diameter of 108 nm, whereas for film thicknesses of 5 and 7 nm, the mean diameter was 128 nm; for 5 and 8 nm, it was 147.9 nm; for 5 and 9 nm, it was 174.3 nm; and for 5 and 10 nm, it was 175 nm. The mean nanoparticle diameter increased linearly as the Ag film thickness increased. However, the specimen with a 10 nm Ag film thickness showed almost the same mean nanoparticle diameter compared to that with a 9 nm Ag film thickness, and the value of the mean diameter reached the saturation at about 175 nm. Furthermore, vertically aligned 40 μm-long Si NWs with a high aspect ratio (~800) were produced via the second MCE process, which lasted for 3 h; Figure 1c shows Si NWs synthesized with film thicknesses of 5 and 8 nm for Au and Ag, respectively. After cutting, the Si NWs were dispersed in a solution of dilute hydrazine and ethanol, in order to prevent surface oxidation. Without dilute hydrazine, the surface of Si nanowires was easily oxidized to be SiO₂ and it made contact resistance between Si nanowires and Au electrodes increased. Thus, the carrier injection from Au electrode to the Si nanowire was disturbed at the interface with high contact resistance, and it caused poor transfer characteristic, as shown in Figure S1 in the Supporting Information.

The microstructure of the synthesized Si NWs was characterized by using a high-resolution transmission electron microscopy (HRTEM). Figure 1d indicates that Si NWs were produced along the $\langle 100 \rangle$ direction and they were single crystals, as evident in the electron diffraction pattern shown in

the inset of Figure 1d. The Si NWs formed through our MCE method had a rough surface, as shown in Figure 1e.

Figure 2a shows an optical microscopy (OM) image of the cylindrical NWs connected to the Au electrodes having a 3 μm gap; the inset is a digital photo image of the specimen, showing the structure of the device, made of Si NWs/Au electrodes/Al₂O₃/PI substrate. The DEP process depends on the dielectric medium, the density of NWs in the medium, the bias on-time, and the strength of the bias field. Here, Al₂O₃ was used as a sacrificial transfer layer and Au electrodes were defined onto it. The electric field used for the DEP process is supposed to be strong between the Au electrodes, whereas no leakage is expected in the other directions. Moreover, Al₂O₃ has a high dielectric constant (9.0–10.1); therefore, the electric field can be directly formed between the Au electrodes.³⁴ The number of Si NWs connected to the Au electrodes per unit of time increased with increasing the density of Si NWs in the dispersion solution, which was used as a dielectric medium. The conditions for the DEP were optimized in order to allow the alignment of one or two Si NWs for 3 s. Figure 2b is the top view OM image of the Si NWs and electrodes transferred on PVP/SiO₂/p⁺⁺ Si wafer, the inset is the cross-sectional SEM image of the device, showing that the cylindrical Si NWs were embedded in the PVP adhesive polymer layer.

Transistors based on Si NWs with different diameters (108, 128, 148, and 174 nm) were fabricated and their electrical properties were measured. From the top view of SEM image and the cross-sectional OM image of the device shown in Figure 2b, the active channel length and width of the sample

were verified. The channel lengths were 3 μm for all the samples, whereas the channel widths were equal to the diameter of the employed Si NWs (Si NWs were assumed to have a two-dimensional structure). The values of the capacitance for the gate dielectric were simulated by Silvaco, along to the diameter of cylindrical Si NWs embedded into the PVP layer (see Figure S2, Supporting Information). The transfer ($I_{\text{ds}}-V_{\text{g}}$) and the output ($I_{\text{ds}}-V_{\text{ds}}$) curve for the p-channel transistor with single Si NWs (148 nm diameter) are shown in Figure 3a and b. An on/off current ratio of 8.17×10^3 was obtained with a threshold voltage (V_{th}) of -2.44 V; the transconductance was measured to be $0.0127 \mu\text{S}$ at a V_{ds} of -5 V. The p-type linear field-effect mobility (μ_{h}) of each device was calculated by using the equation:

$$\mu_{\text{h}} = L/(WC_{\text{d}}V_{\text{ds}})g_{\text{m}} \quad (1)$$

where L is the gap distance between the electrodes, W is the channel width of the device, equal to the diameter of the employed Si NWs, C_{d} represents the capacitance per unit area of the gate dielectric, whose value is 425 pF/cm^2 , and g_{m} is the transconductance. The mobility μ_{h} was determined to be $121.24 \text{ cm}^2/(\text{V s})$. The output characteristic was measured at various V_{g} values from 0 to -20 V in steps of -5 V. I_{ds} increased as the applied V_{g} increased and reached saturation as the V_{ds} increased, which is consistent with the performance of a typical p-channel transistor and implies a good ohmic contact between the Au electrode and the Si NW.

Figure 3c shows the changes in mobility and threshold voltage of the FET as the diameter of the cylindrical Si NW used as channel increases. It was already reported in other papers that the mobility is enhanced by an increase in the diameter of the Si NW, according to the following relation:³⁵

$$\mu \propto d^2 m_{\text{eff}}^{-1.5} \quad (2)$$

where d is the diameter of the Si NW and m_{eff} is the effective mass of a hole. The mobility decreases as the Si NWs become thinner because the huge surface-to-volume ratio causes not only an increase in the phonon–electron wave function overlaps, surface scattering, and defect scattering but also a decrease in the gate coupling.

Si NWs synthesized by the MCE method cause a strong positive surface charge because of the defects and dangling bonds present on the NWs rough surface. This positive surface charge is balanced by a negative charge in the depletion region to accomplish charge neutrality. If the positive surface charge gets stronger, the depletion region becomes larger, so that the effective conduction area is reduced. Since the etching solutions used in the present work had all the same concentration, it is reasonable to assume that the surface roughness of Si NWs with different diameters was identical. Therefore, they had similar values of positive surface charge caused by the surface roughness of NWs, and the effective area of NWs became larger with increasing the Si NW diameter. In other words, the increase in current observed for Si NWs with larger diameters could be caused by the larger cross-sectional area, indicating a reduction in carrier scattering with an increase in diameter. The mobility values were determined to be 80.51, 97.84, 121.24, and $170.95 \text{ cm}^2/(\text{V s})$ for diameters of 108, 128, 148, and 174 nm, respectively. This proportional relationship between mobility and diameter is very similar to that in FET with Si NWs synthesized by VLS.^{35,36}

The threshold voltage is also controlled by the surface roughness of cylindrical Si NWs. If Si NWs were embedded in PVP, the excess carrier concentration in the conduction channel at the interface between PVP and Si NWs was reduced by the presence of OH^- ions, and a scattering effect caused by carrier trapping at the interface occurred. Generally, the positive charge density on the surface of Si NWs increases the conduction of the NWs, whereas the negative charge density decreases the conduction and makes the threshold voltage higher.³⁷ The change of the threshold voltage according to the variation in the Si NW diameter could be induced by the following equation of mobility and conductance in Si NWs:

$$G = \frac{q\mu_{\text{h}}}{L} \int_A n \text{ d}A \quad (3)$$

where G is the conductance, L is the nanowire length, q is the electron charge, μ_{h} is the electron mobility, A is cross sectional area, and n is the electron density for each element.³⁸ As mentioned above, the mobility is proportional to the square of the diameter of the Si NWs. From this relationship, it could be inferred that the conductance is enhanced and the threshold voltage is reduced with an increment in the diameter of the NWs; the threshold voltages were determined to be -7.17 , -4.55 , -2.44 , and 0 V for NWs having diameters of 108, 128, 148, and 174 nm, respectively. The transfer ($I_{\text{ds}}-V_{\text{g}}$) curve obtained for different diameters of Si NWs is shown in Figure S3 (Supporting Information); it was experimentally confirmed that V_{ds} increased and V_{th} was shifted toward 0 V as the Si NW diameter increased.

3. EXPERIMENTAL SECTION

Synthesis of Diameter Controllable Circular Si NWs. Si NWs were synthesized by diameter controllable MCE method from a boron-doped p-type Si (100) wafer with resistivity of $1-10 \Omega\text{-cm}$. The process for synthesis of the Si NWs has been reported in our previous work.³¹ The development point from previous process is that Au on Ag double layer was deposited on Si wafer at the first step to enhance the adhesion property between Si substrate and nanoparticles formed through RTA process instead using Ag single layer. In order to control the diameters of circular Si NWs, the thickness of evaporated Ag layer is changed from 6 to 10 nm in the steps of 1 and 5 nm in the thickness of Au layer was individually deposited on Ag layer by e-beam evaporator. The next processes including annealing process were conducted by the same methods with the previous work. The synthesized circular Si NWs were dispersed in the solution of hydrazine and 99.9% ethanol solution (1:500 v/v).

Formation of Al_2O_3 Sacrificial Layer and Au Electrodes. To prepare the sacrificial layer for this study, slide glass and 15 μm -thick PI substrates were cut into $2 \text{ cm} \times 2.5$ and $3 \text{ cm} \times 3.5$ cm pieces, respectively. The flexible PI substrate wrapped the slide glass and attached on it in order not to be folded or wrinkled. Flexible PI substrate wrapping slide glass was cleaned in 99.9% acetone, 99.9% methanol, and deionized (DI) water by sonication for 10 min. Then, 20 nm-thick Al_2O_3 was deposited on PI substrate by e-beam evaporator with a deposition rate of 0.3 \AA/s . Then, PR solution (AZ5214E) was spin-coated on Al_2O_3 -deposited PI substrate with 500 rpm for 5 s and 2500 rpm for 45 s and baked at $110 \text{ }^\circ\text{C}$ for 50 s in order to form electrodes pattern with a 3 μm gap. The exposure time was confirmed to be 6 s, and PR was developed in developer solution (AZ MIF 300) for 27 s. After rinsing with DI water and drying the specimen with nitrogen gas, a 40 nm-thick Au layer was deposited on the PR pattern formed by photolithography. By stripping the PR pattern with sonication in 99.9% acetone for 2 min and rinsing the specimen with 99.9% methanol and DI water, Au electrodes with a 3 μm gap were defined. Then, the surfaces of the Au electrodes were cleaned by O_2 plasma treatment with 300 W, 50 sccm, 20 Pa, and 5

min of power, flow rate of O₂, working pressure, and operation time, respectively, in order to completely remove the residual on Au electrodes.

Dielectrophoretic Alignment of Si Nanowires on Au Electrodes. DEP alignment method was applied to address prepared Si NWs between Au electrodes. After synthesizing and cutting Si NWs, they were dispersed in the solution of hydrazine and ethanol by sonication for 10 min and the dilute dispersion solution had about 7 × 10⁸ NWs/mL. Through the sonication and dilution processes, the bundle of Si NWs could be separated and individual Si NWs were aligned between Au electrodes by DEP method. After suspending a 4 μL of solution droplet containing Si NWs on Au electrodes, direct current (DC) bias with a frequency of 1 kHz, amplitude of 10 Vpp and a pulse width of 500 μs was applied on the electrodes for 3 s in order for one or two Si NWs to be aligned and connected between electrodes.³⁹

Transfer Layer Formation and Direct Printing. To get high yield of printing and stable device properties, PVP was applied as not only a polymeric adhesive agent but also a dielectric layer for gate insulator. First of all, 10% PVP solution and a cross-linking agent, poly(melamine-co-formaldehyde) (PMCF), in propylene glycolmonomethyl ether acetate (PGMEA) was coated onto thermally oxidized p⁺⁺ Si substrate with 300 nm-thick SiO₂ layer. PVP layers spin-coated on Si substrate with the condition of 500 rpm for 5 s and 5000 rpm for 120 s were softly baked at 110 °C for 10 min. A Si NWs-addressed PI substrate at the second step was separated from slide glass for imprinting and transferring process. Separated PI substrate was flipped over and stamped onto softly baked PVP layer at the third step and heated up from 110 to 140 °C with an increasing rate of 2 °C/min. Au electrodes and addressed Si NWs were transferred into PVP layer by detaching the Al₂O₃-deposited PI substrate and fabrication of circular Si NW FET was completed by baking PVP in vacuum at 175 °C for 1 h.

4. CONCLUSION

In summary, we fabricated a FET with Si NWs synthesized through the MCE process and we investigated the dependence of the electrical properties, such as mobility and threshold voltage, on the NW diameter. Cylindrical Si NWs were synthesized as previously reported, using a Au and Ag double layer instead of a Ag single layer. For the fabrication of the Si NW-based FET, cylindrical Si NWs with diameters of 108, 128, 148, and 174 nm were connected between Au electrodes using the DEP process and then decal-printed on PVP-coated on p⁺⁺ Si substrate with 300 nm-thick SiO₂. Findings show that the mobility of devices increased while the threshold voltage decreased with increasing the Si NW diameter, because the surface-to-volume ratio decreased, whereas the defects characterizing the rough surface were not influential.

■ ASSOCIATED CONTENT

Supporting Information

Electrical property (transfer curve) of Si NW FET without hydrazine treatment. Additional information for simulated capacitance values and transfer characteristic of Si NW FET according to various diameters of Si nanowire. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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Author Contributions

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Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This research was supported by WCU program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology [R32-20031] and by the LG Display academic industrial cooperation program.

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